Michael Scholl

Department of Electrical Engineering, Eindhoven University of Technology

contact@mscholl.eu LinkedIn GitHub

Education

Eindhoven University of Technology Aug 2024 – Aug 2027
BSc Electrical Engineering (GPA: 9.2/10), Honors Academy

Technical Skills

Analog & Mixed-Signal: Cadence Virtuoso, Spectre, Verilog-A, LTspice
Digital & FPGA: Verilog, Verilator (C/C++ testbenches), Vivado, PYNQ-Z2, RISC-V
Software & Modeling: Python (PyTorch, NumPy), C, MATLAB/Simulink, Git
PCB & CAD: Altium Designer, Fusion 360, SolidWorks
Languages: German (native), English (C1), Spanish (B2), Dutch (A2)

Projects

Digitally Assisted Pipelined ADC | *Cadence Virtuoso, Spectre, Verilog-A, Python* Sep 2026 – Oct 2026
- Designed a low-power open-loop residue amplifier at transistor level for a 12-bit, 100 MS/s pipelined ADC
- Corrected the amplifier's nonlinearity digitally with a cubic fit, raising ENOB from 9.3 to 11.6 of 12 bits

ANN vs. SNN Inference on RISC-V (FPGA) | *Verilog, Verilator, Vivado, PyTorch* Sep 2026 – Present
- Benchmarking artificial vs. spiking neural network inference on edge devices using a PicoRV32 RISC-V core
- MNIST and ECG arrhythmia classification with custom Vivado bitstreams running on PYNQ-Z2 FPGA

Experience

Teaching Assistant Sep 2026 – Present
Electronic Circuits 2
- Supervise analog circuit tutorials and LTspice simulation hours for the oscillator laboratory

Researcher & Developer Sep 2025 – Jun 2026
Honors Academy, Team NaviSense
- Led development of an indoor navigation app for visually impaired users and pitched its business case

Flight Electronics Engineer Oct 2025 – May 2026
Student Rocketry Team VOID
- Designed a flight computer PCB in Altium and wrote embedded C drivers for its flight-critical sensor interfaces

Teaching Assistant Feb 2026 – Apr 2026
Computer Architecture
- Guided FPGA synthesis and deployment of RTL designs (Verilog), bridging digital theory and implementation

Additional Training

Eindhoven Semiconductor Summer School (ESSS) Aug 2026 – Sep 2026
- Selected for the programme co-organized by ASML, NXP, TSMC, imec, ASM, and SmartPhotonics
- Benchmarked 2D CFETs for Ångström-era transistors under Prof. Ye Wang (TU/e)

Eindhoven–South Korea Future Chips Academy Jun 2026 – Jul 2026
- Presented on EUV lithography and the step-and-scan scanner, supervised by Prof. Sung-Min Lee

Point-of-Care Photonic Biosensor | *Course Project, TU/e* Apr 2026 – Jun 2026
- Developed a conceptual photonic chip (microring + photonic-crystal cavities) in a multidisciplinary team
- Led sensor integration, including cost analysis and surface regeneration for reuse

Computer Vision Methods (Czech Technical University) Oct 2025 – Jun 2026
- Graduate course (grade A): CNNs, Transformers, SIFT/RANSAC, visual tracking, Structure-from-Motion